Currentless Data Transmission Mechanism Within Processor Architectures Utilizing Aligned Trapped Electrons and Fractional Capacitance Discharge Piezo-Induction Transistors for Substantially Improved Transistor Proximity

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Introduction

Independent of limitations on transistor proximity in processor design related to heat density (this issue has already been addressed) limits exist for the absolute proximity of one transistor to another related to the tendency of current to arc from one transistor to the next. Reducing the amount of current flowing through the processor to the maximum extent possible is a longstanding goal in developing next-generation processors with improved transistor proximity.

Abstract

The combination of multiple novel concepts may enable the development of a new type of processor that utilizes qualitatively distinct types of semiconductor transistors designed to operate upon the principle of Net Zero Current Flow Switching with a novel transistor charge modality.

Semiconductor transistors presently operate according to the principle of fully charging and discharging a transistor with each cycle, with a longstanding goal of the development of these transistors being increasing the ephemerality of capacitance of the transistors. While increasing this ephemerality would remain a goal in this new design, the full discharge of the capacitance of each transistor would not only be unnecessary, but undesirable in the context of this novel concept. Rather than designing transistors that fully discharge with each cycle, these novel transistors would discharge by a margin of perhaps 0.2% of their full capacity and would thus alternate between 100% charge and 99.8% of charge.

Rather than current flowing through wires connecting these transistors, a series of electrons in a series of ion traps would occupy the spaces ordinarily occupied by wires. These electrons would be stationary and would not leave their respective ion traps during the switching process.

When a transistor that is upstream is switched "on," i.e. its charge is increased to 100%, downstream transistors, given that they have a piezoelectric property, may experience current induction as the result of changes in ambient Coulomb forces (ibid. Coulomb Force Line Piezo-Fabrication of Processors as Alternative to Photofabrication.)

If Coulomb forces may be used to bring about electrical induction in order to support the initial formation of coherent transistors on the angstrom-scale, it stands to reason that this general principle should allow for the level of charge in

such a transistor to be modified in accordance with more subtle projections of Coulomb Force.

The only point at which current would be required to power such system would be at the processor pins. Beyond this point, current could be induced from one transistor to the next using static electrons as the mode of signal conveyance. As no current would be flowing and as there would be little relative difference between the level of charge of "on" and "off" transistors, arcing between transistors would be unlikely to occur, even when these transistors have as little as 0.85nm of space separating them.

Conclusion

The only limiting factor in such a system would be the ephemerality of capacitance of the transistors as well as the scaling of the ion trap system. As the speed of computation within such a system would far exceed that of conventional designs, entire computing systems would need to be built upon similar principles to prevent bottlenecks in data flow.